Phison Electronics Corporation

Embedded SSD Series

Automotive PCIe NVMe SSD Specification

(PS5021-E21T + Kioxia 112L 3D TLC)

MPT560

Version 2.4

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Revision History

Revision	Draft Date	History	Author
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2.3	2024/06/07	Revise Power consumption	Eleven Tseng
2.4	2024/09/20	1. Revise PS4 (<2.5Mw) in Product Overview page 2. Revise Notes3 in MAX Current page 3. Revise warranty policy	Eleven Tseng

Product Overview

- **Product Series: MPT560**
- **Capacity**
  - 64GB, 128GB, 256GB, 512GB, 1024GB
- **Form Factor**
  - BGA type 1620, 16 mm x 20 mm
  - M.2 type 2230, 22mm x 30mm
- **PCIe Express Base Specification**
  - Gen 4 x 4 lanes
  - NVMe 1.4
  - PCI Express Base 4.0
  - PCI Express M.2 Specification Revision 4.0, Version 1.0
- **Performance**[1]
  - Read: up to 3650MB/s
  - Write: up to 2900MB/s
- **Reliability**
  - MTBF > 2 million hours (Mean Time Between Failure)
  - UBER < 1 sector per 10^{16} bits read (Uncorrectable Bit Error Rate)
- **Package Compliant**
  - RoHS
  - MSL3
- **Voltage Supply Rails**
  - BGA type 1620
    - P1=2.5V
    - P2=1.2V
    - P3=0.85V
  - M.2 type 2230 = 3.3V
- **Power Saving Modes (Optional)**
  - PS0/ PS1/ PS2/ PS3/ PS4 (< 2.5W)
  - Support APST
  - Support ASPM
  - Support L1.2
- **Endurance: Total Bytes Written (TBW)**
  - Up to 1341TB for 1024GB
- **Temperature Range**[2]
  - Automotive Grade 2: -40°C ~ 105°C
  - Industrial Grade: -40°C ~ 85°C
- **Features Support List:**
  - Self-monitoring, analysis, and reporting technology (SMART)
  - Host-controlled thermal management
  - Power loss protection
  - End to end data path protection
  - Thermal throttling
  - LDPC + RAID ECC
  - SmartRefresh™
  - Support HMB(Host Memory Buffer)[3] (option support)
  - Support TCG OPAL(option support)[4]
  - RPMB
  - Boot Partition

NOTES:

1. For more details on Performance, please refer to Chapter 2.
2. The operation temperature means the case temperature.
3. Win10 (version 1809) and above supports HMB (Host Memory Buffer) function.
4. BGASSD 1620 type doesn't support PSID QR Code screen (if needed please contact to us)

Product Series Naming Rule

M	P	T	5	6	0
Product Type	**Interface**	**Solution Type**	**Generation**	**Flash type**	**Reserved**
- M: Embedded SSD for Mission Criterial Application	- S: SATA - P: PCIe	- D: DRAM - T: DRAM-Less	- 5: PS5021-E21TI	- 6: Kioxia 112L	

Package Inking

BGA Size	Grade	Part Number	Dimension	BGA	Flash mode	Density
1620	Automotive Grade 2 (-40°C ~ 105°C)	ESE3D211-64GA	16x20x1.15mm	291 Ball	1-CH	64GB
		ESE3D222-X28A	16x20x1.15mm	291 Ball	2-CH	128GB
		ESE3D243-256A	16x20x1.15mm	291 Ball	4-CH	256GB
		ESE3D244-512A	16x20x1.35mm	291 Ball	4-CH	512GB
		ESE3D247-M24A	16x20x1.65mm	291 Ball	4-CH	1024GB
	Industrial (-40°C ~ 85°C)	ESE3D211-64GI	16x20x1.15mm	291 Ball	1-CH	64GB
		ESE3D222-X28I	16x20x1.15mm	291 Ball	2-CH	128GB
		ESE3D243-256I	16x20x1.15mm	291 Ball	4-CH	256GB
		ESE3D244-512I	16x20x1.35mm	291 Ball	4-CH	512GB
		ESE3D247-M24I	16x20x1.65mm	291 Ball	4-CH	1024GB

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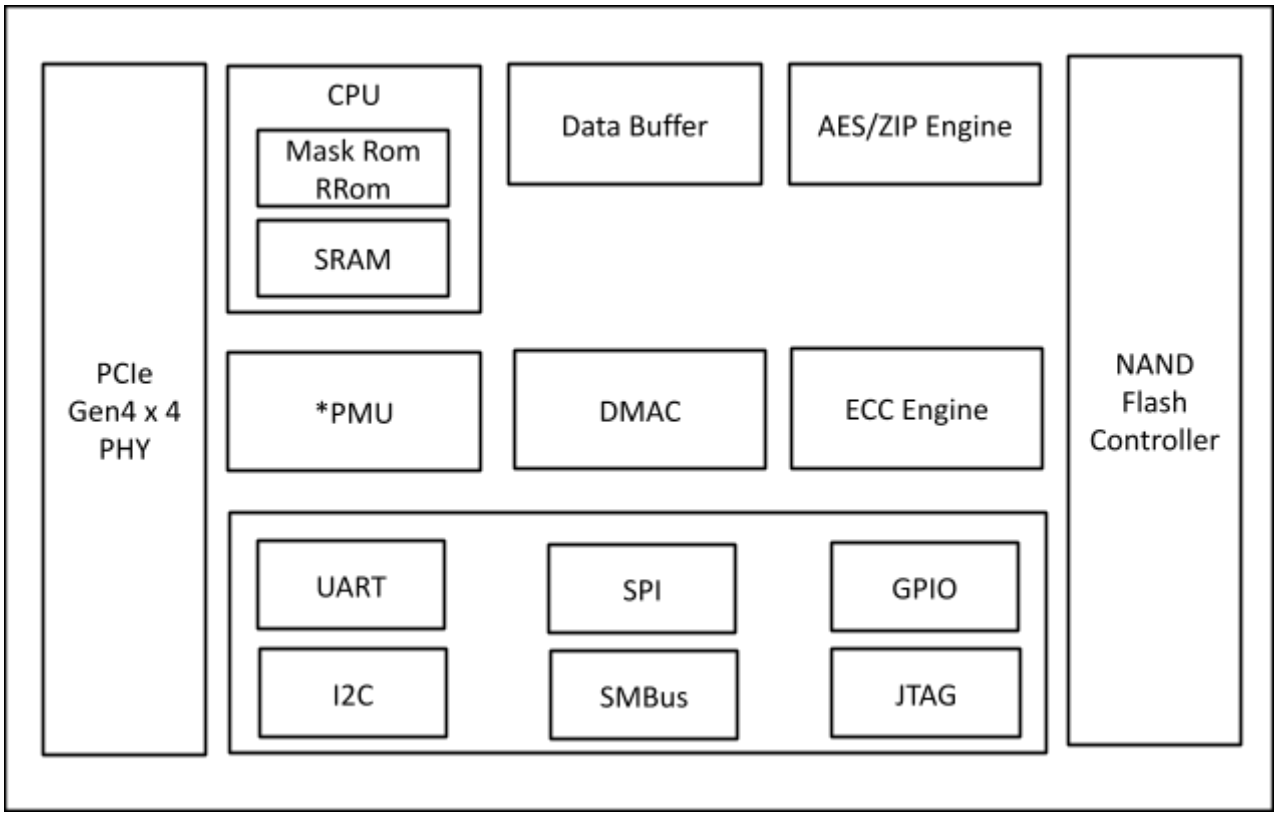
1. INTRODUCTION

1.1. General Description

Phison MPT560 (PS5021-E21TI) 1620 BGA SSD delivers all the advantages of flash drive technology with PCIe Gen 4x4 interface in an embedded BGA form factor. The MPT560 (PS5021-E21TI) 1620 BGA SSD could provide the capacity range from 64GB to 1024GB. It is estimated to reach up to 3650 MB/s read as well as 2900 MB/s write sequential performance. The MPT560 (PS5021-E21TI) 1620 BGA SSD throughput is capable of saturating Gen 4x4 host interface. Moreover, the power consumption of MPT560 (PS5021-E21TI) 1620 BGA SSD is much lower than traditional hard drives, making it the best embedded solution for new platforms.

1.2. Controller Block Diagram



*PMU: Power management unit

Figure 1-1 Controller Block Diagram

1.3. Flash Management

1.3.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, MPT560 (PS5021-E21TI) 1620 PCIe BGA SSD applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.3.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Phison provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3.3. Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

1.3.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no

longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

1.3.5. S.M.A.R.T.

S.M.A.R.T., an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by S.M.A.R.T., users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, S.M.A.R.T. can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

1.3.6. Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/ Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.3.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgradable when new features are added, compatibility issues are fixed, or read/write performance gets improved. Phison has its own secure firmware. The firmware codes are all RSA signed and are checked by download and boot ROM. Any unauthorized firmware cannot be loaded into our SSD.

1.4. Advanced Device Security Features

1.4.1. Secure Erase

Secure Erase is a standard NVMe format command and will make all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

1.5. SSD Lifetime Management

1.5.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity)] / [WAF]

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

1.5.2. Media Wear Indicator

Actual life indicator reported by SMART Attribute byte index [5], Percentage Used, recommends User to replace drive when reaching to 100%.

1.5.3. Read Only Mode (End of Life)

When drive is aged by cumulated program/erase cycles, media worn-out may cause increasing numbers of later bad block. When the number of usable good blocks falls outside a defined usable range, the drive will notify Host through AER event and Critical Warning to enter Read Only Mode to prevent further data

corruption. User should start to replace the drive with another one immediately.

1.6. An Adaptive Approach to Performance Tuning

1.6.1. Throughput

Based on the available space of the disk, MPT560 (PS5021-E21TI) 1620 PCIe BGA SSD will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, MPT560 (PS5021-E21TI) 1620 PCIe BGA SSD will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.6.2. SLC Caching

MPT560 (PS5021-E21TI) 1620 PCIe BGA SSD's firmware design currently adopts dynamic caching to deliver better performance for better endurance and consumer user experience.

2. PRODUCT SPECIFICATIONS

- ~~**Product: MPT560**~~

- **Capacity**
  - 64GB, 128GB, 256GB, 512GB, 1024GB
  - Support 32-bit addressing mode
- **Electrical/Physical Interface**
  - PCIe Interface
  - Compliant with NVMe 1.4
  - PCIe Express Base ver. 4.0
  - PCI Express M.2 Specification Revision 4.0, Version 1.0
  - PCIe Gen 4 x 4 lane & backward compatible to PCIe Gen 3, PCIe Gen 2 and Gen 1
  - Support up to QD 128 with queue depth of up to 64K
  - Support power management
- **Supported NAND Flash**
  - Support up to 16 Flash Chip Enables (CE) within a single design
  - Support 8-bit I/O NAND Flash
  - Support Toggle 2.0, Toggle 3.0 and Toggle 4.0 interface
    - ◊ Kioxia 112-Layers 3D TLC
- **ECC Scheme**
  - MPT560 (PS5021-E21TI) 1620 BGA SSD applies the LDPC + RAID ECC algorithm.
- **Sector Size Support**
  - 512byte
  - 4KB
- **UART/GPIO**
- **Voltage Rails**
  - BGASSD type 1620
    - P1=2.5V

  - P2=1.2V
  - P3=0.85V
- M.2 type 2230 = 3.3V

- **Support SMART and TRIM commands**

- **LBA Range**
  - IDEMA standard

Table 2-1 User Capacity and Addressable Sectors

Capacity	512 Bytes/Sector		4K Bytes/Sector	
	Number of Total LBA	**User Available Bytes**	**Number of Total LBA**	**User Available Bytes**
64GB	125,045,424	64,023,257,088	15,630,678	64,023,257,088
128GB	250,069,680	128,035,676,160	31,258,710	128,035,676,160
256GB	500,118,192	256,060,514,304	62,514,774	256,060,514,304
512GB	1,000,215,216	512,110,190,592	125,026,902	512,110,190,592
1024GB	2,000,409,264	1,024,209,543,168	250,051,158	1,024,209,543,168

- **Performance**

Kioxia 112Layers 3D TLC (1200MT/s)
PS0 (Full Speed Mode)

Table 2-2 Performance

Capacity	Flash Structure	CE#	Performance			
			Sequential		Random	
			Read (MB/s)	**Write (MB/s)**	**Read (IOPS)**	**Write (IOPS)**
64GB	64GB x 1	1	660	250	30K	53K
128GB	64GB x 2	2	1400	510	60K	120K
256GB	64GB x 4	4	2950	1000	110K	245K
512GB	64GB x 8	8	3650	1900	220K	450K
1024GB	64GB x 16	16	3650	2900	380K	500K

NOTES:
1. Performance may differ according to flash configuration, use condition, environment and platform.
2. Use CrystalDiskMark 7.0.0 with QD8T1, 1GB range for sequential read/write test
3. Use IOmeter v1.1.0 with QD32T16, 1GB range for 4KB random read/write test.

4. Performance specification is under that Thermal Throttling has not worked yet.
5. CPU: AMD Ryzen 7 5800X 8-Core Processor
6. Operating System: Windows 10 Professional (x64)
7. Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

- **TBW (Terabytes Written)**

Table 2-3 TBW

Capacity	TBW	DWPD
64GB	70	1
128GB	85	0.606
256GB	248	0.885
512GB	661	1.180
1024GB	1341	1.196

NOTES:

1. TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3000. It may differ according to flash configuration and platform configuration.
2. DWPD (Drive Write Per Day) is calculated based on 3-year lifetime.
   DWPD = TBW / (365 days x 3 years x User Capacity)
3. The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

- **Thermal Throttling**

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. PS5021-E21T is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- Purpose of Thermal Throttling:

  In order to keep the optimal performance in the safe range of the temperature.
- Thermal sensors:

  We have on-die thermal sensor (inside the controller and NAND flash) to detect temperature.

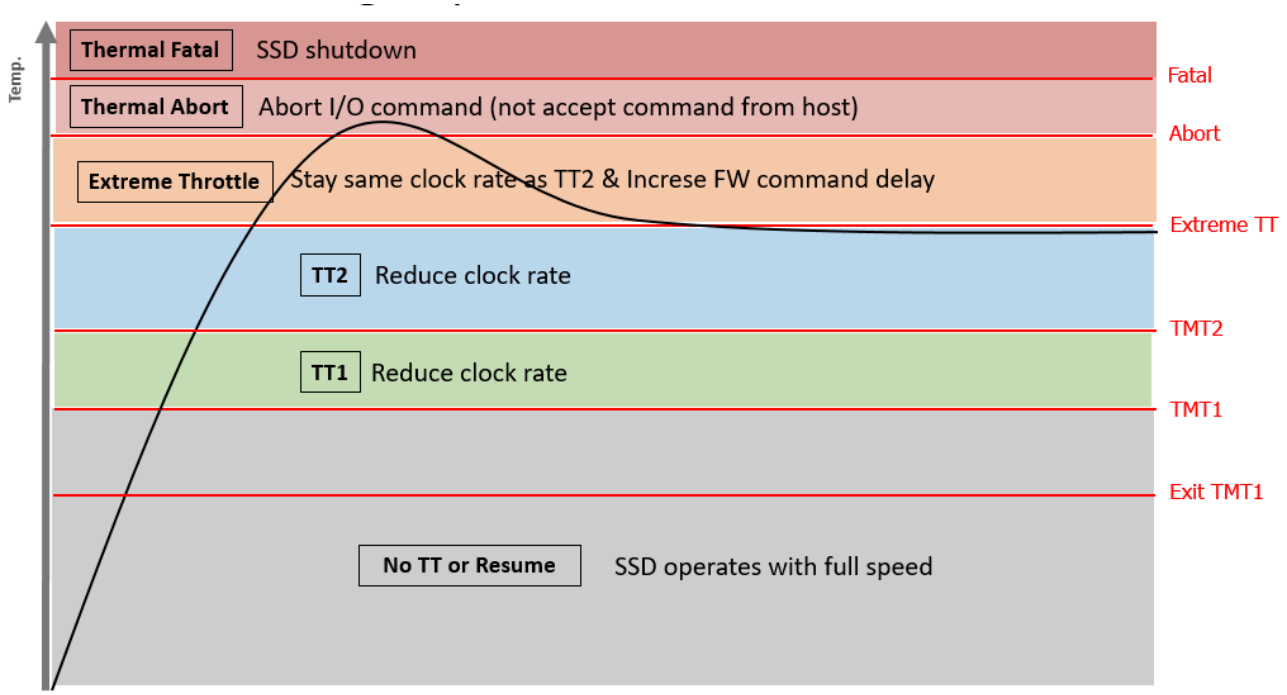


Figure 2-1 Thermal Throttling by On-die Thermal Sensor

- **TCG Opal 2.0 (Option)**

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of

data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

TCG Opal 2.0 Main Features:

- AES 256-bitHardware Self Encryption
- Deploy Storage Device & Take Ownership: The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device: LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device: unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life: erasure of data within one or more

- **Autonomous Power State Transition(Option)**

Device to support multiple power states. APST supports states where there is reduced power equating to slower performance or where the device is temporarily sleeping in a non-operational state and then woken up on activity. APST allows the transition between operational state (PS0/1/2) and non-operational states (PS3/4) automatically. Host can configure power state as below table:

Table 2-4 APST

Initial Power States	ITPS	ITPT (ms) *
PS0	PS3	100
PS1	PS3	100
PS2	PS3	100
PS3	PS4	9,900

Notes:

1. Idle Transition Power State (ITPS): Transfer from Initial Power States to other Power States.
2. Idle Time Prior to Transition (ITPT): The waiting time that Initial Power States transfers to other Power States when device is idle.

- **Active State Power Management(Option)**

Active-state power management (ASPM) is a power management mechanism for PCI Express devices. It is an autonomous hardware-based, active state mechanism that enables power savings even when the connected components are in the fully active state. Link Power Management State (L0, L1, L1.1, L1.2) can be controlled by ASPM. PCI Express defines the following Link power management states:

- L0: Active state
- L0s: A low resume latency, energy saving "standby" state.
- L1: Higher latency, lower power "standby" state.

- L1.1: Lite-energy-saving state.
- L1.2: Deep-energy-saving state.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. MTBF

MTBF, Mean Time between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on Telcorida methodology. Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Table 3-1 MTBF

Capacity	MTBF
64GB	2 million hours
128GB	
256GB	
512GB	
1024GB	

3.2. Certification & Compliance

- RoHS
- WHQL
- PCI Express Base 4.0
- UNH-IOL NVM Express Logo

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage (BGA Type 1620)

Table 4-1 Supply Voltage

Parameter	Rating			
Operating Voltage	Specification	Min.	Nom.	Max.
	Flash Core	+2.45V	+2.5V	+2.75V
	Flash IO supply	+1.16V	+1.2V	+1.26V
	Controller Core	+0.80V	+0.85V	+0.88V
Rise Time (Max/Min)	1.2ms/0.8ms			
Fall Time (Max/Min)	Note[4]			

NOTES:
1. Minimum time between power removed from SSD (V_{CC} < 500 mW) and power re-applied to the drive.
2. It shall be driven down Vcc to below 0.5V and stay low for at least 1ms before Vcc power up.
3. The Min. Off Time may differ according to power solution used.
4. Please follow PCI Express M.2 Specification: BGA SSD Voltage Supply Power-off Sequencing.

4.2. Power Consumption (BGA Type 1620)

Table 4-2 Kioxia 112L 3D TLC (1200MT/s) Power Consumption of each power state in mW

Capacity	Flash Structure	CE#	Read			Write			PS3	PS4
			PS0	PS1	PS2	PS0	PS1	PS2		
64GB	64GB x 1	1	1,750	1,465	1,250	1,550	1,250	1,200	50	2.5
128GB	64GB x2	2	2,065	1,800	1,250	1,650	1,350	1,200	50	2.5
256GB	64GB x 4	4	2,900	2,000	1,350	2,200	1,700	1,200	50	2.5
512GB	64GB x 8	8	3,200	2,200	1,300	2,650	1,700	1,200	50	2.5
1024GB	64GB x 16	16	3,500	2,100	1,300	3,500	1,800	1,200	50	2.5

NOTES:
1. Power consumption is estimated with the condition under ambient temperature @25°C.
2. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
3. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.

Table 4-3 Kioxia 112L 3D TLC (1200MT/s) PS0 (Full Speed Mode) MAX Current in mA

Capacity	Flash Structure	CE#	PWR1 Max (mA)	PWR2 Max (mA)	PWR3 Max (mA)
64GB	64GB x 1	1	300	430	1,500
128GB	64GB x2	2	650	650	1,500
256GB	64GB x 4	4	970	1,000	1,500
512GB	64GB x 8	8	1,000	1,130	1,500
1024GB	64GB x 16	16	1,100	1,260	1,500

NOTES:

1. Power consumption is estimated with the condition under ambient temperature @25°C.
2. The Max value of power consumption is achieved based on 100% conversion efficiency.
3. Max current is estimated under burst performance

4.3. Supply Voltage (M.2 Type 2230)

Table 4-4 Supply Voltage

Parameter	Rating		
Operating Voltage	Min.	Nom.	Max.
	+3.135V	+3.3V DC	+3.465V
Rise Time (Max/Min)	1.2ms/0.8ms		
Fall Time (Max/Min)	Note[4]		

NOTES:
1. Minimum time between power removed from SSD (V_{CC} < 500 mW) and power re-applied to the drive.
2. It shall be driven down Vcc to below 0.5V and stay low for at least 1ms before Vcc power up.
3. The Min. Off Time may differ according to power solution used.
4. Please follow PCI Express M.2 Specification: BGA SSD Voltage Supply Power-off Sequencing.

4.4. Power Consumption (M.2 Type 2230)

Table 4-5 Kioxia 112L 3D TLC (1200MT/s) Power Consumption in mW

Capacity	Flash Structure	CE#	Read	Write
64GB	64GB x 1	1	2050	1880
128GB	64GB x2	2	2460	2070
256GB	64GB x 4	4	3570	2670
512GB	64GB x 8	8	4000	3600
1024GB	64GB x 16	16	4230	4520

NOTES:
1. The measured power voltage of M.2 SSD is 3.3V.
2. Measurement environment: Room temperature: 20~25 °C, humidity: 40~60%RH, DC+3.3V condition.
3. Power consumption may differ according to flash configuration, use condition, environment and platform configuration.

4.5. Idle Power Consumption (M.2 Type 2230)

Table 4-6 Kioxia 112L 3D TLC (1200MT/s) Idle Power Consumption in mW

Capacity	Flash Structure	CE #	Idle
64GB	64GB x 1	1	1500
128GB	64GB x2	2	1500
256GB	64GB x 4	4	1500
512GB	64GB x 8	8	1500
1024GB	64GB x 16	16	1500

[Notes]

1. Idle power consumption is measured at idle state with no write/read operation.
2. The measured power voltage of M.2 SSD is 3.3V.
3. Measurement environment: Room temperature: 20~25 °C, humidity: 40~60%RH, DC+3.3V condition.
4. Power consumption may differ according to flash configuration, use condition, environment and platform configuration.

5. INTERFACE

5.1. BGA type 1620 Pin Assignment/Descriptions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	A
B	DNU	DNU		DNU		DNU		1V8_REG			DNU		DNU		DNU		DNU	DNU	B
C	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	FLASH_RZQ	DNU	DNU	DNU	DNU	GND	DNU	DNU	DNU	C
D				REFCLKP	REFCLKN	GND	PERSTN	CLKREQB	PWR_1	PWR_1	GND	XEXTRSTB	DIAG1	DNU	DNU				D
E	GND	GND	GND	GND	GND	GND	GND	DNU	PWR_1	PWR_1	GND	DNU	DIAG0	GND	GND	DNU	DNU	DNU	E
F				PERP0	PERN0	GND								DNU	GND				F
G	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	G
H				PETP0	PETN0		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	PLN				H
J	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	J
K				PERP1	PERN1		GND	GND	GND	GND	GND	GND		DNU	PLA				K
L	GND	GND	GND	GND	GND		DNU	DNU	DNU	DNU	DNU	DNU		GND	GND	DNU	DNU	DNU	L
M				PETP1	PETN1		DNU	DNU	GND	GND	DNU	DNU		DNU	DNU				M
N	GND	GND	GND	GND	GND		DNU	DNU	DNU	DNU	DNU	DNU		GND	GND	DNU	JTAG_TCK	JTAG_TMS	N
P				PERP2	PERN2		GND	GND	GND	GND	GND	GND		DNU	DNU				P
R	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	XGPIO0	DNU	R
T				PETP2	PETN2		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		DNU	DNU				T
U	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA	U
V				PERP3	PERN3									DNU	DNU				V
W	GND	GND	GND	GND	GND	GND	LED/DAS	DNU	PWR_1	PWR_1	GND	DNU	DNU	GND	GND	DNU	DNU	DNU	W
Y				PETP3	PETN3	GND	DNU	DNU	PWR_1	PWR_1	GND	DNU	GND	DNU	DNU				Y
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	CTL_RZQ	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU	AA
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AB
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 5-1 BGA type 1620 Pin Assignment

Table 5-1 BGA type 1620 Pin Description

Pin Name	BGA 291	Pin Type	Description	IO Voltage
UART/GPIO				
XGPIO0	R17	I	Debug only	1.8V
DIAG1	D13	I	Debug only	1.8V
DIAG0	E13	O	Debug only	1.8V
SMB_CLK	U17	I/O	Debug only	1.8V
SMB_DATA	U18	I/O	Debug only	1.8V
JTAG_TCK	N17	I/O	Debug only	1.8V
JTAG_TMS	N18	I/O	Debug only	1.8V
XEXTRSTB	D12	-	Debug only	1.8V
1V8_REG	B8	-	Debug only	1.8V
PCIe Interface Signals				
PERP0	F4	I/O	PCIe TX/RX Differential signals defined by the PCI Express Card Electromechanical Specification.	--
PERN0	F5			
PERP1	K4			
PERN1	K5			
PERP2	P4			
PERN2	P5			
PERP3	V4			
PERN3	V5			
PETP0	H4			
PETN0	H5			
PETP1	M4			
PETN1	M5			
PETP2	T4			
PETN2	T5			
PETP3	Y4			
PETN3	Y5			
REFCLKP	D4	I	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Card Electromechanical Specification.	--
REFCLKN	D5	I		--
PERSTN	D7	I	PCIe Reset is a functional reset to the card as defined by the PCI Express Mini Card Electromechanical Specification	1.8V
CLKREQB	D8	I/O	Clock Request is a reference clock request signal as defined by the PCI Express Mini Card Electromechanical Specification; Also used by L1 PM Substates.	1.8V

Optional Signals				
FLASH_RZQ	C10	I	Flash Calibration REF RESISTENCE	-
CTL_RZQ	AA10	I	CTL Calibration REF RESISTENCE	-
PLA	K15	O	Power Loss Acknowledge	1.8V
PLN	H15	I	Power Loss Notification	1.8V
SSD Specific Signals				
LED/DAS#	W7	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3V
Power Supply Signals				
PWR_1	D9	I	+2.5 V source	2.5V
	D10			
	E9			
	E10			
	W9			
	W10			
	Y9			
	Y10			
PWR_2	R7	I	+1.2 V source	1.2V
	R8			
	R11			
	R12			
	T7			
	T8			
	T11			
	T12			
	U7			
	U8			
	U11			
	U12			
PWR_3	G7	I	+0.85 V source	0.85V
	G8			
	G11			
	G12			
	H7			
	H8			
	H11			

	H12			
	J7			
	J8			
	J11			
	J12			
Pin Name	BGA 291	Description		

GND	C1	GND
	C2	
	C3	
	C4	
	C5	
	C15	
	D6	
	D11	
	E1	
	E2	
	E3	
	E4	
	E5	
	E6	
	E7	
	E11	
	E14	
	E15	
	F6	
	F15	
	G1	
	G2	
	G3	
	G4	
	G5	
	G9	
	G10	
	G14	
	G15	
	H9	
GND	H10	GND
	H14	
	J1	
	J2	
	J3	
	J4	
	J5	

GND	J9	GND
	J10	
	J14	
	J15	
	K7	
	K8	
	K9	
	K10	
	K11	
	K12	
	L1	
	L2	
	L3	
	L4	
	L5	
	L14	
	L15	
	M9	
	M10	
	N1	
	N2	
	N3	
	N4	
	N5	
	N14	
	N15	
	P7	
	P8	
	P9	
	P10	
	P11	
	P12	
	R1	
	R2	
	R3	
	R4	
	R5	

	R9	
	R10	
	R14	
	R15	
	T9	
	T10	
	U1	
	U2	
	U3	
	U4	
	U5	
	U9	
	U10	
	U14	
	U15	
	W1	
	W2	
	W3	
	W4	
	W5	
	W6	
	W11	
	W14	
	W15	
	Y6	
	Y11	
	Y13	
	AA1	
	AA2	
	AA3	
	AA4	
	AA5	
	AA14	
	AA15	

DNU	A1	Do not use. Manufacturing purpose only
	A2	
	A4	
	A6	
	A8	
	A11	
	A13	
	A15	
	A17	
	A18	
DNU	B1	Do not use. Manufacturing purpose only
	B2	
	B4	
	B6	
	B11	
	B13	
	B15	
	B17	
	B18	
	C6	
	C7	
	C8	
	C9	
	C11	
	C12	
	C13	
	C14	
	C16	
	C17	
	C18	
	D14	
	D15	
	E8	
	E12	
	E16	
	E17	
	E18	

DNU	F14	Do not use. Manufacturing purpose only
	G16	
	G17	
	G18	
	J16	
	J17	
	J18	
	K14	
	L7	
	L8	
	L9	
	L10	
	L11	
	L12	
	L16	
	L17	
	L18	
	M7	
	M8	
	M11	
	M12	
	M14	
	M15	
	N7	
	N8	
	N9	
DNU	N10	Do not use. Manufacturing purpose only
	N11	
	N12	
	N16	
	P14	
	P15	
	R16	
	R18	
	T14	
	T15	
	U16	

	V14	
	V15	
	W8	
	W12	
	W13	
	W16	
	W17	
	W18	
	Y7	
	Y8	
	Y12	
	Y14	
	Y15	
	AA6	
	AA7	
	AA8	
	AA9	
	AA11	
	AA12	
	AA13	
	AA16	
	AA17	
	AA18	
	AB1	
	AB2	
	AB4	
	AB6	
	AB8	
	AB11	
	AB13	
	AB15	
	AB17	
	AB18	
	AC1	
	AC2	
	AC4	
	AC6	

	AC8	
	AC11	
	AC13	
	AC15	
	AC17	
	AC18	

5.2. M.2 type 2230 Pin Assignment/Descriptions

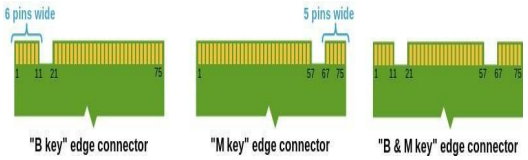


Figure 5-2 M.2 PCIe SSD Pin Assignment

Table 5-1 defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.0 of the PCI-SIG.

Table 5-2 Pin Assignment and Description of MPT560 (PS5021-E21TI) M.2 2230

Pin #	PCIe Pin	Description
1	CONFIG_3 = GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No Connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	PLN# (I)(0/3.3V)	Power Loss Notification
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source

19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	PLA_S3# (O)(0/3.3V)	Power Loss Acknowledge; Open Drain with pull-up on platform
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.

54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	Module Key
61	Module Key M	Module Key
62	Module Key M	Module Key
63	Module Key M	Module Key
64	Module Key M	Module Key
65	Module Key M	Module Key
66	Module Key M	Module Key
67	N/C	No Connect
68	SUSCLK(32KHz)(I)(0/3.3V)	No connect
69	N/C	CONFIG_1 = No connect
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	CONFIG_2 = Ground

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test
15h	Namespace Attachment
18h	Keep Alive

Table 6-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 6-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-4 Identify Controller Data Structure

Bytes	Description	Default Value
01:00	PCI Vendor ID (VID)	0x1987
03:02	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	Serial Number (SN)	SN
63:24	Model Number (MN)	Model Number

Bytes	Description	Default Value
71:64	Firmware Revision (FR)	FW Name
72	Recommended Arbitration Burst (RAB)	0x4
75:73	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x0
77	Maximum Data Transfer Size (MDTS)	0x6
79:78	Controller ID (CNTLID)	0x0
83:80	Version (VER)	0x10400
87:84	RTD3 Resume Latency (RTD3R)	0x186A0
91:88	RTD3 Entry Latency (RTD3E)	0x4C4B40
95:92	Optional Asynchronous Events Supported (OAES)	0x0
99:96	Controller Attributes (CTRATT)	0x2
101:100	Read Recovery Levels Supported (RRLS)	0x0
110:102	Reserved	0x00
111	Controller Type (CNTRLTYPE)	0x1
127:112	FRU Globally Unique Identifier (FGUID)	0x00
129:128	Command Retry Delay Time 1 (CRDT1)	0x0
131:130	Command Retry Delay Time 2 (CRDT2)	0x0
133:132	Command Retry Delay Time 3 (CRDT3)	0x0
239:134	Reserved	0x00
255:240	Refer to the NVMe Management Interface Specification for Definition	0x00
257:256	Optional Admin Command Support (OACS)	0x17
258	Abort Command Limit (ACL)	0x3
259	Asynchronous Event Request Limit (AERL)	0x7
260	Firmware Updates (FRMW)	0x12
261	Log Page Attributes (LPA)	0x1E
262	Error Log Page Entries (ELPE)	0xFE
263	Number of Power States Support (NPSS)	0x4
264	Admin Vendor Specific Command Configuration (AVSCC)	0x1
265	Autonomous Power State Transition Attributes (APSTA)	0x1
267:266	Warning Composite Temperature Threshold (WCTEMP)	0x17D
269:268	Critical Composite Temperature Threshold (CCTEMP)	0x17F
271:270	Maximum Time for Firmware Activation (MTFA)	0x64
275:272	Host Memory Buffer Preferred Size (HMPRE)	0x0 (HMB off) Depend on Disk Size(HMB on)
279:276	Host Memory Buffer Minimum Size (HMMIN)	0x0(HMB off) Depend on Disk Size(HMB on)
295:280	Total NVM Capacity (TNVMCAP)	By capacity
311:296	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	Replay Protected Memory Block Support (RPMBS)	0x1F0002
317:316	Extended Device Self-test Time (EDSTT)	0x1E
318	Device Self-test Options (DSTO)	0x0
319	Firmware Update Granularity (FWUG)	0x4
321:320	Keep Alive Support (KAS)	0x0
323:322	Host Controlled Thermal Management Attributes (HCTMA)	0x1
325:324	Minimum Thermal Management Temperature (MNTMT)	0x111
327:326	Maximum Thermal Management Temperature (MXTMT)	0x170
331:328	Sanitize Capabilities (SANICAP)	0xA0000002

Bytes	Description	Default Value
335:332	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)	0x400
337:336	Host Memory Maximum Descriptors Entries (HMMAXD)	0x10
339:338	NVM Set Identifier Maximum (NSETIDMAX)	0x0
341:340	Endurance Group Identifier Maximum (ENDGIDMAX)	0x0
342	ANA Transition Time (ANATT)	0x0
343	Asymmetric Namespace Access Capabilities (ANACAP)	0x0
347:344	ANA Group Identifier Maximum (ANAGRPMAX)	0x0
351:348	Number of ANA Group Identifiers (NANAGRPID)	0x0
355:352	Persistent Event Log Size (PELS)	0x60
511:356	Reserved	0x00
512	Submission Queue Entry Size (SQES)	0x66
513	Completion Queue Entry Size (CQES)	0x44
515:514	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	Number of Namespaces (NN)	0x1
521:520	Optional NVM Command Support (ONCS)	0xD7
523:522	Fused Operation Support (FUSES)	0x0
524	Format NVM Attributes (FNA)	0x0
525	Volatile Write Cache (VWC)	0x7
527:526	Atomic Write Unit Normal (AWUN)	0xFF
529:528	Atomic Write Unit Power Fail (AWUPF)	0x0
530	NVM Vendor Specific Command Configuration (NVSCC)	0x1
531	Reserved	0x0
533:532	Atomic Compare & Write Unit (ACWU)	0x0
535:534	Reserved	0x00
539:536	SGL Support (SGLS)	0x0
543:540	Maximum Number of Allowed Namespaces (MNAN)	0x0
767:544	Reserved	0x00
1023:768	NVM Subsystem NVMe Qualified Name (SUBNQN)	nqn.2020-11.org.nvmexpress:uuid: (SN)
1791:1024	Reserved	0x00
2047:1792	Refer to the NVMe over Fabrics specification	0x00
2079:2048	Power State 0 Descriptor (PSD0)	
Bit[255:184]	Reserved	0x00
Bit[183:182]	Active Power Scale (APS)	0x0
Bit[181:179]	Reserved	0x0
Bit[178:176]	Active Power Workload (APW)	0x0
Bit[175:160]	Active Power (ACTP)	0x0
Bit[159:152]	Reserved	0x0
Bit[151:150]	Idle Power Scale (IPS)	0x0
Bit[149:144]	Reserved	0x0
Bit[143:128]	Idle Power (IDLP)	0x0
Bit[127:125]	Reserved	0x0
Bit[124:120]	Relative Write Latency (RWL)	0x0
Bit[119:117]	Reserved	0x0
Bit[116:112]	Relative Write Throughput (RWT)	0x0
Bit[111:109]	Reserved	0x0
Bit[108:104]	Relative Read Latency (RRL)	0x0
Bit[103:101]	Reserved	0x0
Bit[100:96]	Relative Read Throughput (RRT)	0x0
Bit[95:64]	Exit Latency (EXLAT)	0x0

Bytes	Description	Default Value
Bit[63:32]	Entry Latency (ENLAT)	0x0
Bit[31:26]	Reserved	0x0
Bit[25]	Non-Operational State (NOPS)	0x0
Bit[24]	Max Power Scale (MPS)	0x0
Bit[23:16]	Reserved	0x0
Bit[15:0]	Maximum Power (MP)	0x1F4
2111:2080	Power State 1 Descriptor (PSD1)	
Bit[255:184]	Reserved	0x00
Bit[183:182]	Active Power Scale (APS)	0x0
Bit[181:179]	Reserved	0x0
Bit[178:176]	Active Power Workload (APW)	0x0
Bit[175:160]	Active Power (ACTP)	0x0
Bit[159:152]	Reserved	0x0
Bit[151:150]	Idle Power Scale (IPS)	0x0
Bit[149:144]	Reserved	0x0
Bit[143:128]	Idle Power (IDLP)	0x0
Bit[127:125]	Reserved	0x0
Bit[124:120]	Relative Write Latency (RWL)	0x1
Bit[119:117]	Reserved	0x0
Bit[116:112]	Relative Write Throughput (RWT)	0x1
Bit[111:109]	Reserved	0x0
Bit[108:104]	Relative Read Latency (RRL)	0x1
Bit[103:101]	Reserved	0x0
Bit[100:96]	Relative Read Throughput (RRT)	0x1
Bit[95:64]	Exit Latency (EXLAT)	0x0
Bit[63:32]	Entry Latency (ENLAT)	0x0
Bit[31:26]	Reserved	0x0
Bit[25]	Non-Operational State (NOPS)	0x0
Bit[24]	Max Power Scale (MPS)	0x0
Bit[23:16]	Reserved	0x0
Bit[15:0]	Maximum Power (MP)	0xF0
2143:2112	Power State 2 Descriptor (PSD2)	
Bit[255:184]	Reserved	0x00
Bit[183:182]	Active Power Scale (APS)	0x0
Bit[181:179]	Reserved	0x0
Bit[178:176]	Active Power Workload (APW)	0x0
Bit[175:160]	Active Power (ACTP)	0x0
Bit[159:152]	Reserved	0x0
Bit[151:150]	Idle Power Scale (IPS)	0x0
Bit[149:144]	Reserved	0x0
Bit[143:128]	Idle Power (IDLP)	0x0
Bit[127:125]	Reserved	0x0
Bit[124:120]	Relative Write Latency (RWL)	0x2
Bit[119:117]	Reserved	0x0
Bit[116:112]	Relative Write Throughput (RWT)	0x2
Bit[111:109]	Reserved	0x0
Bit[108:104]	Relative Read Latency (RRL)	0x2
Bit[103:101]	Reserved	0x0
Bit[100:96]	Relative Read Throughput (RRT)	0x2
Bit[95:64]	Exit Latency (EXLAT)	0x0

Bytes	Description	Default Value
Bit[63:32]	Entry Latency (ENLAT)	0x0
Bit[31:26]	Reserved	0x0
Bit[25]	Non-Operational State (NOPS)	0x0
Bit[24]	Max Power Scale (MPS)	0x0
Bit[23:16]	Reserved	0x0
Bit[15:0]	Maximum Power (MP)	0xBE
2175:2144	Power State 3 Descriptor (PSD3)	
Bit[255:184]	Reserved	0x00
Bit[183:182]	Active Power Scale (APS)	0x0
Bit[181:179]	Reserved	0x0
Bit[178:176]	Active Power Workload (APW)	0x0
Bit[175:160]	Active Power (ACTP)	0x0
Bit[159:152]	Reserved	0x0
Bit[151:150]	Idle Power Scale (IPS)	0x0
Bit[149:144]	Reserved	0x0
Bit[143:128]	Idle Power (IDLP)	0x0
Bit[127:125]	Reserved	0x0
Bit[124:120]	Relative Write Latency (RWL)	0x3
Bit[119:117]	Reserved	0x0
Bit[116:112]	Relative Write Throughput (RWT)	0x3
Bit[111:109]	Reserved	0x0
Bit[108:104]	Relative Read Latency (RRL)	0x3
Bit[103:101]	Reserved	0x0
Bit[100:96]	Relative Read Throughput (RRT)	0x3
Bit[95:64]	Exit Latency (EXLAT)	0x7D0
Bit[63:32]	Entry Latency (ENLAT)	0x1770
Bit[31:26]	Reserved	0x0
Bit[25]	Non-Operational State (NOPS)	0x1
Bit[24]	Max Power Scale (MPS)	0x1
Bit[23:16]	Reserved	0x0
Bit[15:0]	Maximum Power (MP)	0x1F4
2207:2176	Power State 4 Descriptor (PSD4)	
Bit[255:184]	Reserved	0x00
Bit[183:182]	Active Power Scale (APS)	0x0
Bit[181:179]	Reserved	0x0
Bit[178:176]	Active Power Workload (APW)	0x0
Bit[175:160]	Active Power (ACTP)	0x0
Bit[159:152]	Reserved	0x0
Bit[151:150]	Idle Power Scale (IPS)	0x0
Bit[149:144]	Reserved	0x0
Bit[143:128]	Idle Power (IDLP)	0x0
Bit[127:125]	Reserved	0x0
Bit[124:120]	Relative Write Latency (RWL)	0x4
Bit[119:117]	Reserved	0x0
Bit[116:112]	Relative Write Throughput (RWT)	0x4
Bit[111:109]	Reserved	0x0
Bit[108:104]	Relative Read Latency (RRL)	0x4
Bit[103:101]	Reserved	0x0
Bit[100:96]	Relative Read Throughput (RRT)	0x4
Bit[95:64]	Exit Latency (EXLAT)	0x9C40

Bytes	Description	Default Value
Bit[63:32]	Entry Latency (ENLAT)	0x2710
Bit[31:26]	Reserved	0x0
Bit[25]	Non-Operational State (NOPS)	0x1
Bit[24]	Max Power Scale (MPS)	0x1
Bit[23:16]	Reserved	0x0
Bit[15:0]	Maximum Power (MP)	0x32
…	(N/A)	0
3071:3040	Power State 31 Descriptor (PSD31)	0
3107:3072	Vendor Specific (VS)	0x00
3109:3108	PLP Supported	0x8001
4095:3110	Vendor Specific (VS)	0x00

6.3. SMART Attributes

Table 6-5 SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[203:202]	2	Temperature Sensor 2
[205:204]	2	Temperature Sensor 3
[207:206]	2	Temperature Sensor 4
[209:208]	2	Temperature Sensor 5
[211:210]	2	Temperature Sensor 6
[213:212]	2	Temperature Sensor 7
[215:214]	2	Temperature Sensor 8
[219:216]	4	Thermal Management Temperature 1 Transition Count
[223:220]	4	Thermal Management Temperature 2 Transition Count
[227:224]	4	Total Time For Thermal Management Temperature 1
[231:228]	4	Total Time For Thermal Management Temperature 2
[511:232]	280	Reserved

7. PHYSICAL DIMENSION

7.1. BGA type 1620

- Package: 16mm (x-axis) x 20mm (y-axis) / 0.8mm (Ball Pitch)

Table 7-1 BGA SSD Physical Dimensions and Weight

Capacity	Height (mm)	Width (mm)	length (mm)	Weight (gram)
64GB	1.15	16	20	0.67
128GB	1.15			0.67
256GB	1.15			0.67
512GB	1.35			0.84
1024GB	1.65			1

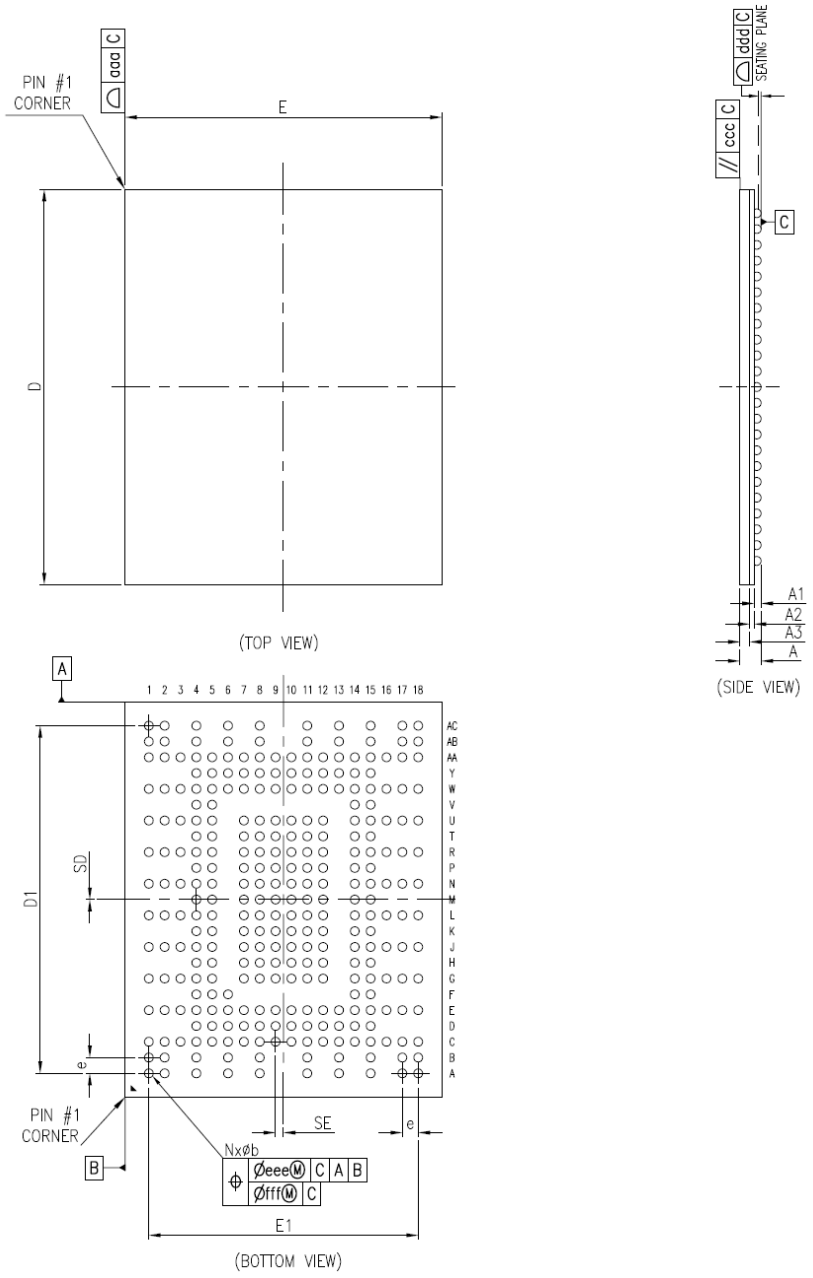


Figure 7-1 BGA type 1620 Package Outline Drawing

Table 7-2 Package Specification (Kioxia 112Layers 3D TLC x1/x2/x4 solution)

LY No.PS-MK-291-56001-**	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.95	1.07	1.15
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2		0.22	
MOLD THICKNESS	A3		0.50	
BODY SIZE	D		20	
	E		16	
BALL DIAMETER			0.45	
BALL OPENING			0.40	
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e		0.80	
BALL COUNT	N		291	
EDGE BALL CENTER TO CENTER	D1		17.60 BSC.	
	E1		13.60 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.00 BSC.	
	SE		0.40 BSC.	
JEDEC(REF)			MO-216(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	ccc		0.20	
COPLANARITY	ddd		0.20	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.08	

NOTES:

1. All dimensions are in mm.
2. Ball designation is per JEP95, SECTION 3, SPP-010.
3. Fiducial Markings (Missing Fiducial location is A1 Corner Indicator).
4. A1 Triangle (orientation can vary and is non-critical).
5. DIM b is measured at the maximum solder ball diameter, parallel to primary datum Z.

Table 7-3 Package Specification (Kioxia 112Layers 3D TLC x8 solution)

LY No.PS-MK-291-56001-**	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.15	1.27	1.35
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2		0.22	
MOLD THICKNESS	A3		0.70	
BODY SIZE	D		20	
	E		16	
BALL DIAMETER			0.45	
BALL OPENING			0.40	
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e		0.80	
BALL COUNT	N		291	
EDGE BALL CENTER TO CENTER	D1		17.60 BSC.	
	E1		13.60 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.00 BSC.	
	SE		0.40 BSC.	
JEDEC(REF)			MO-216(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	ccc		0.20	
COPLANARITY	ddd		0.20	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.08	

NOTES:

6. All dimensions are in mm.
7. Ball designation is per JEP95, SECTION 3, SPP-010.
8. Fiducial Markings (Missing Fiducial location is A1 Corner Indicator).
9. A1 Triangle (orientation can vary and is non-critical).
10. DIM b is measured at the maximum solder ball diameter, parallel to primary datum Z.

Table 7-4 Package Specification (Kioxia 112Layers 3D TLC x16 solution)

LY No.PS-MK-291-56001-**	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.45	1.57	1.65
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2		0.22	
MOLD THICKNESS	A3		1.00	
BODY SIZE	D		20	
	E		16	
BALL DIAMETER			0.45	
BALL OPENING			0.40	
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e		0.80	
BALL COUNT	N		291	
EDGE BALL CENTER TO CENTER	D1		17.60 BSC.	
	E1		13.60 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.00 BSC.	
	SE		0.40 BSC.	
JEDEC(REF)			MO-216(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	ccc		0.20	
COPLANARITY	ddd		0.20	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.08	

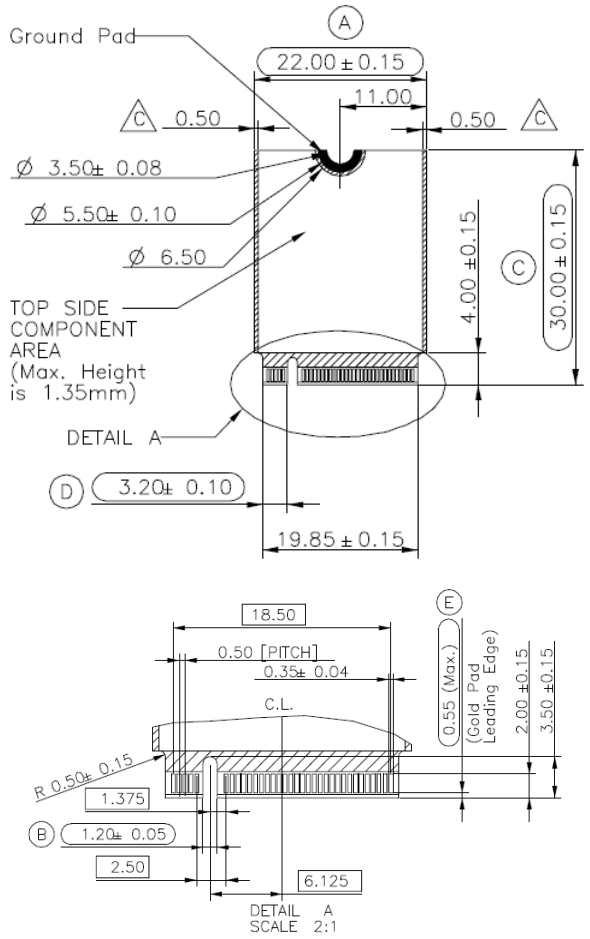
NOTES:

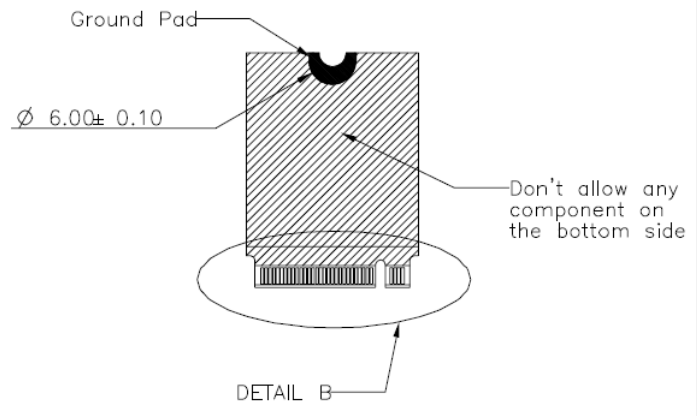
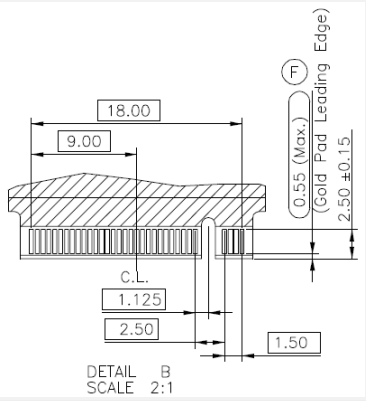
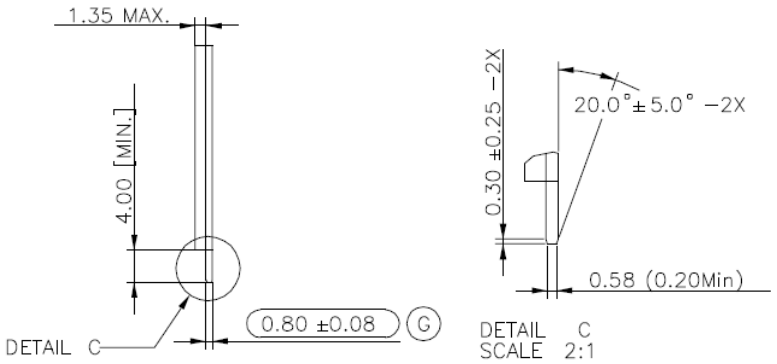
1. All dimensions are in mm.
2. Ball designation is per JEP95, SECTION 3, SPP-010.
3. Fiducial Markings (Missing Fiducial location is A1 Corner Indicator).
4. A1 Triangle (orientation can vary and is non-critical).
5. DIM b is measured at the maximum solder ball diameter, parallel to primary datum Z.

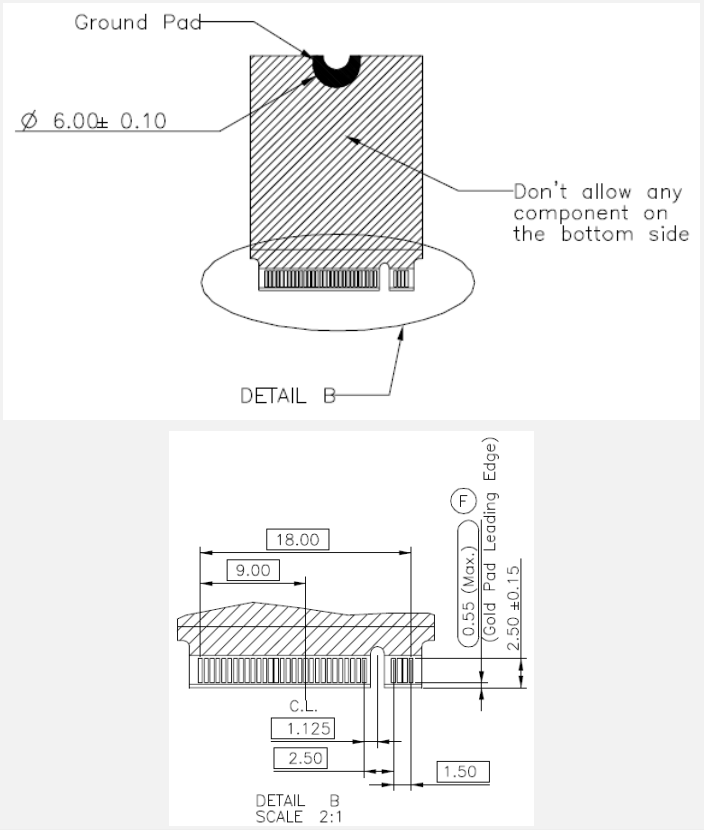
7.2. M.2 type 2230

Table 7-5 M.2 type 2230 Physical Dimensions

Capacity(GB)	Height (mm)	Width (mm)	Length (mm)
64	2.15±0.08	22±0.15	30±0.15
128			
256			
512			
1024			

View Direction	Diagram
Top	

Bottom	 
Side	

Bottom	

Notes :
1. = Max Component Height
2. = No Component
3. = No Component / Signal Vias / Signal Copper / Printing
4.General Tolerance ±0.15mm
5. are critical dimensions

Figure 7-2 M.2 type 2230 Package Outline Drawing

8. APPLICATION NOTES

8.1. Wafer Level Chip Scale Packaging (WLCSP) Handling Precautions

There are a lot of components assembled on a single SSD device. Please handle the drive with care especially when it has any WLCSP (Wafer Level Chip Scale Packaging) components such as PMIC, thermal sensor or load switch. WLCSP is one of the packaging technologies that is widely adopted for making smaller footprints, but any bumps or scratches may damage those ultrasmall parts so gentle handling is strongly recommended.

⚠ **DO NOT DROP SSD**

⚠ **INSTALL SSD WITH CARE**

⚠ **STORE SSD IN A PROPER PACKAGE**

8.2. M Key M.2 SSD Assembly Precautions

M Key M.2 SSD (Figure 1) is only compatible to M Key (Figure 2) socket. As shown in Use Case 2, misuse may cause severe damages to SSD including burn-out.

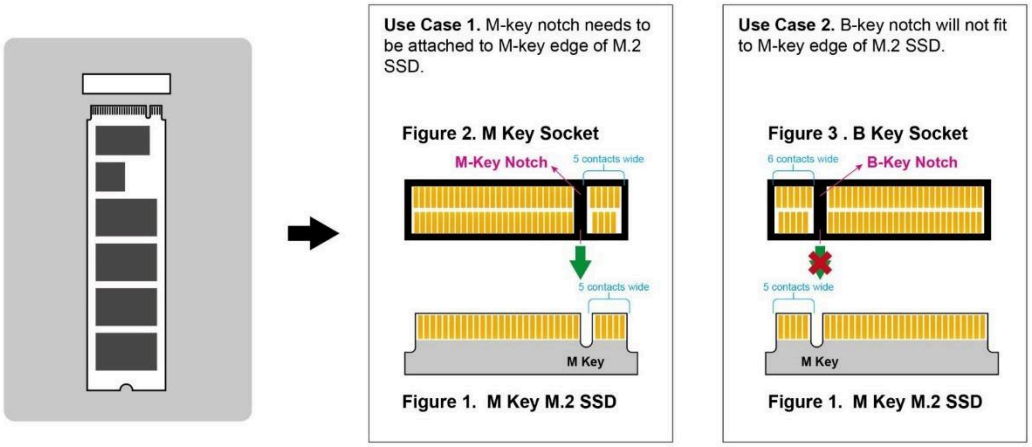


Figure 8-1 M Key M.2 Assembly Precautions

9. PRODUCT WARRANTY POLICY

For any other products manufactured and supplied by Phison (“Phison Products”), Phison hereby certify that in the event Phison Product does not conform to the specification for (A) a period instructed by Phison or mutually agreed by Phison and the customer in writing or (B) the period ending on the date at which customer’s use of a Phison Product exceeds Phison Product’s total Terabytes Written as recorded by or derived from Phison Product’s S.M.A.R.T. Attribute, including but not limited to, Phison Product’s drive life is used up in accordance with the S.M.A.R.T. Attribute, whichever occurs earlier(“Warranty Period”) and such inconformity is confirmed by Phison to be solely attributable to Phison, Phison agrees to repair or replace the nonconforming Phison Product, free of charge.

Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

(1) alternation, modification, improper use, misuse or excessive use of Phison Product;
(2) failure to comply with Phison’s instructions;
(3) Phison’s compliance with or use of the instructions, technologies, designs, specifications, devices, materials, components, parts, software and firmware provided, instructed or approved by Buyer (including any of its parents, subsidiaries, affiliates, suppliers, subcontractors or downstream customers);
(4) combination of Phison Product with other materials, components, parts, goods, hardware, firmware or software not supplied by Phison;
(5) any claim brought by a third party who is commonly known as intellectual property right assertion entity or patent troll;
(6) NAND flash itself or NAND flash which is embedded into Phison Products;
(7) Phison’s compliance with general industry standards;
(8) other error or failure not solely attributable to Phison’s cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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THREATEN LIFE, INJURY, HEALTH, LOSS OF SIGNIFICANT AMOUNT OF MONEY ("CRITICAL USE"), AND BUYER AND USER HEREBY ASSUMES ALL RISK OF ANY CRITICAL USE OF PHISON PRODUCT.

10. REFERENCE

The following table is to list out the standards that have been adopted for designing the product.

Table 10-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at sales@phison.com or support@phison.com.
M.2	http://www.pcisig.com
PCI Express Base 4.0	https://www.pcisig.com/specifications/pciexpress/base4/
NVM Express Specification Rev. 1.4	http://www.nvmexpress.org/
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a

11. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 11-1 List of Terminology

Term	Definitions
ATTO	Commercial performance benchmark application
DDR	Double data rate (SDRAM)
ASPM	Active states power management
APST	Autonomous power state transition
LBA	Logical block addressing
MB	Mega-byte
GB	Giga-byte
TB	Tera-byte
MTBF	Mean time between failures
PCIe	Pci express / peripheral component interconnect express
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk