Phison Electronics Corporation

PS5012-E12 M.2 2280 FIPS 140-2 Phison Feature with ECPM13.1/ ECPM15.0 Specification

Version 1.1

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Revision History

Revision	Date	History	Author
1.0	2022/06/28	First Release	Lester Chang
1.1	2024/09/27	Add BiCS5 information	Lester Chang

This specification is based on firmware version ECPM1x.x and is subject to change without notice. Any deviation on following firmware revisions will not be updated unless the deviation is more than 5%

Product Overview

- **Capacity**
  - 256GB up to 2048GB
- **Form Factor**
  - E12 M.2 2280-D2-M
- **PCIe Interface**
  - PCIe Gen3 x 4
- **Compliance**
  - NVMe 1.3
  - PCI Express Base 3.1
- **Flash Interface**
  - Transfer rate up to 667 MBps
  - Up to 4pcs of BGA132 flash
- **Performance[1]**
  - Read: up to 3400 MB/s
  - Write: up to 3100 MB/s
- **Reliability**
  - Mean Time Between Failure (MTBF) 1.8 million hours
  - Uncorrectable Bit Error Rate (UBER) < 1 sector per 10^{16} bits read
- **Advanced Flash Management**
  - Advanced Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
  - Firmware Update
- **Power Management**
  - Support APST
  - Support ASPM
  - Support L1.2
- **Power Consumption[2]**
  - Idle < 350mW
  - L1.2 < 5 mW
- **Temperature Range**
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
  - Operation airflow: 800 LFM at 35C ambient
- **RoHS compliant**
- **Features Support List:**
  - End to end data path protection
  - Thermal throttling
  - SmartECC™
  - SmartRefresh™
  - TCG OPAL
  - FIPS 140-2 lv2 certified: certificate number #3758
  - Cigent Feature with ECPM13.1/ECPM15.0

Notes:

1. Refer to Chapter 2 for more details
2. Refer to Chapter 4, Section 4.2 Power Consumption for more details.

Performance and Power Consumption

Form Factor	Capacity	Flash Configuration (3D NAND/BGA Package)	Performance[1]			
			CrystalDiskMark		IOMeter	
			Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
M.2 2280 Double Side (BiCS4)	E12 256GB	64GB x 4, 8CE, 256Gb DDP	3300	1300	210K	320K
	E12 512GB	128GB x 4, 16CE, 256Gb QDP	3400	2500	420K	625K
	E12 1024GB	256GB x 4, 32CE, 256Gb ODP	3400	3100	640K	680K
	E12 2048GB	512GB x 4, 32CE, 512Gb ODP	3400	3000	635K	685K
M.2 2280 Double Side (BiCS5)	E12 256GB	128GB x 2, 4CE, 512Gb DDP	1900	1100	100K	280K
	E12 512GB	128GB x 4, 8CE, 512Gb DDP	3300	2300	200K	550K
	E12 1024GB	256GB x 4, 16CE, 512Gb QDP	3300	3100	400K	600K
	E12 2048GB	512GB x 4, 32CE, 512Gb ODP	3300	3000	640K	630K

Capacity	Flash Configuration (BGA Package)	Power Consumption[2]			
		Read (W)	Write (W)	PS3 (mW)	PS4 (mW)
E12 256GB	64GB x 4, 8CE, 256Gb DDP BGA132, BiCS4	5.0	3.1	16	2
E12 512GB	128GB x 4, 16CE, 256Gb QDP BGA132, BiCS4	5.1	4.5	16	2
E12 1024GB	256GB x 4, 32CE, 256Gb ODP BGA132, BiCS4	5.3	5.2	21	2
E12 2048GB	512GB x 4, 32CE, 512Gb ODP BGA132, BiCS4	5.3	5.7	22	2
E12 256GB	128GB x 2, 4CE, 512Gb DDP BGA132, BiCS5	3.7	2.0	16	2
E12 512GB	128GB x 4, 8CE, 512Gb DDP BGA132, BiCS5	5.2	2.1	16	2
E12 1024GB	256GB x 4, 16CE, 512Gb QDP BGA132, BiCS5	5.5	2.0	20	2
E12 2048GB	512GB x 4, 32CE, 512Gb ODP BGA132, BiCS5	5.5	2.2	33	2

NOTES:

1. Performance is measured based on the following conditions:
   A. CrystalDiskMark 6.0.0, 1GB range, QD=32, Thread=1
   B. IOMeter, 1GB range, 4K data size, QD=32
2. Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark with the conditions described in 1(A).

FIPS 140-2 certificate #3758

Module	Capacity	Hardware P/N and Version	FW Version
PS5012-E12 M.2 2280 NVME NAND Flash SSD	E12 256GB	PSE12F-M2280-256G-V01	ECPM13.1
	E12 512GB	PSE12F-M2280-512G-V01	ECPM13.1
	E12 1024GB	PSE12F-M2280-1024G-V01	ECPM13.1
	E12 2048GB	PSE12F-M2280-2048G-V01	ECPM13.1
	E12 256GB	PSE12F-M2280-256G-V02	ECPM15.0
	E12 512GB	PSE12F-M2280-512G-V02	ECPM15.0
	E12 1024GB	PSE12F-M2280-1024G-V02	ECPM15.0
	E12 2048GB	PSE12F-M2280-2048G-V02	ECPM15.0

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1. INTRODUCTION

1.1. General Description

Phison PS5012-E12 M.2 2280 delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. PS5012-E12 M.2 2280 offers a wide range capacity up to 2048GB and its performance can reach up to 3400 MB/s[1] (for read) and 3100 MB/s[1] (for write) based on 32CE NAND flash with 512MB/1GB/2GB DDR4[2]. Moreover, the power consumption of PS5012 M.2-E12 2280 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

NOTE:

1. Achieved by 1024GB SSD with external 1GB DDR4 at FOB (fresh-out-of-box) state on CrystalDiskMark v6.0.0.
2. The choice of DDR4 depends on drive capacity; DDR size≧0.1% of SSD capacity.

1.2. Controller Block Diagram

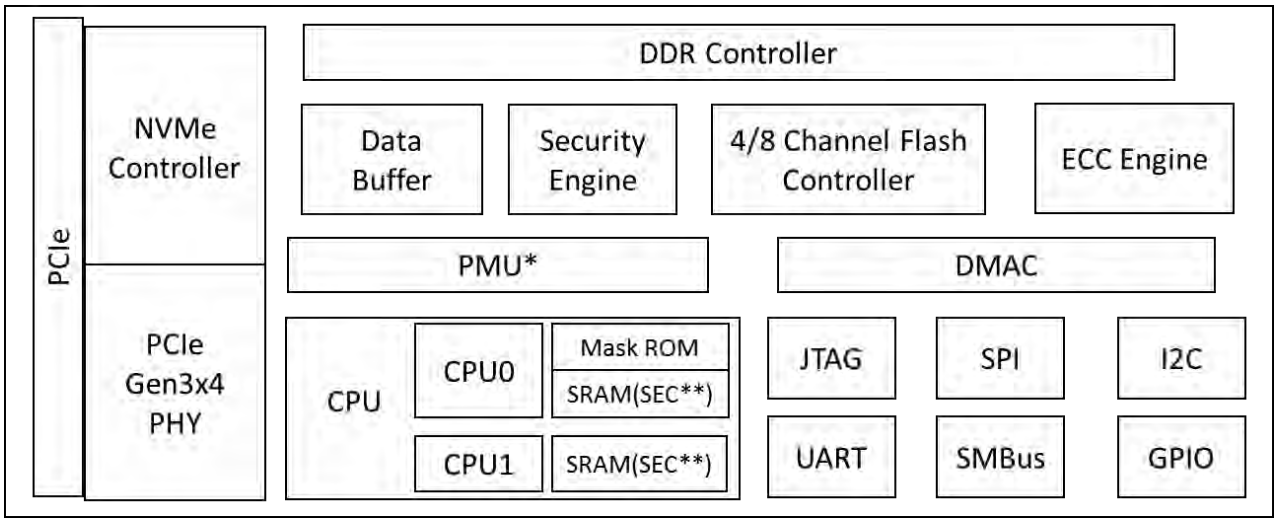


Figure 1-1 PS5012 Controller Block Diagram

NOTE:

1. PMU: Power Management Unit
2. SEC: Single bit Error Correct

1.3. Product Block Diagram

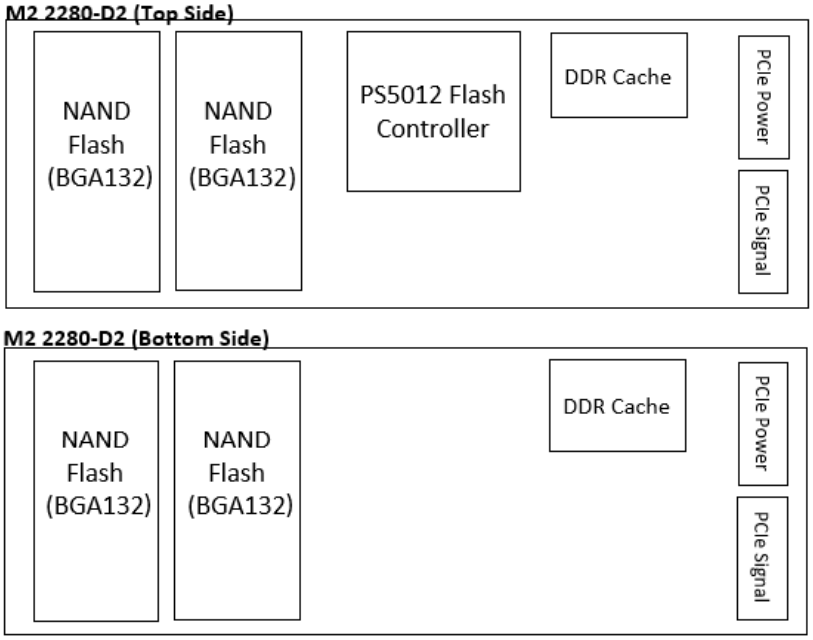


Figure 1-2 PS5012 M.2 2280 Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS5012-E12 PCIe SSD applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occurred during read process, to ensure data being read correctly, as well as to protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

1.4.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

1.4.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.4.6. Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.4.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.4.8. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. PS5012 is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

Current version:

Item	Content
Smart reporting temperature	Flash normalized case temperature
Reference of temp. reading	On-board thermal sensor, Controller on-die thermal sensor
tmt1 threshold	68℃ per Smart reported
tmt2 threshold	70℃ per Smart reported
Protect threshold	80℃ per Smart reported
Protect controller threshold	115℃ from on-die thermal sensor
Fatal threshold	120℃ from on-die thermal sensor
Resume performance threshold	64℃ per Smart reported
Temperature polling frequency	Every 1 sec
TMT1_state impact	±10% CE
TMT2_state impact	-20% CE

1.5. Advanced Device Security Features

1.5.1. Physical Presence SID (PSID)

Physical Presence SID (PSID) is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

1.5.2. Sanitize Operation

Drive Security Type	AES-256 Encryption	Sanitize Operation (command)			TCG Commands		IEEE 1667
		Overwrite	Block Erase	Crypto Erase	PSID Revert Process	Instant Security Erase	Windows eDrive
FIPS (TCG OPAL)	Yes	Disable	Disable	Disable	Yes	Via TCG Revert (PSID)	Disable

1.6. SSD Lifetime Management

1.6.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity) / WAF

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

1.6.2. Media Wear Indicator

Actual life indicator reported by SMART Attribute byte index [5], Percentage Used, recommends User to replace drive when reaching to 100%.

1.6.3. Read Only Mode (End of Life)

When drive is aged by cumulated program/erase cycles, media worn- out may cause increasing numbers of later bad block. When the number of usable good blocks falls outside a defined usable range, the drive will notify Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. User should start to replace the drive with another one immediately.

1.7. An Adaptive Approach to Performance Tuning

1.7.1. Throughput

Based on the available space of the disk, PS5012-E12 will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, PS5012 will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.7.2. Predict & Fetch

Normally, when the Host tries to read data from the PCIe SSD, the PCIe SSD will only perform one read action after receiving one command. However, PS5012 applies ***Predict & Fetch*** to improve the read speed. When the host issues sequential read commands to the PCIe SSD, the PCIe SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

1.7.3. SLC Caching

PS5012's firmware design currently adopts dynamic caching to deliver better performance for better endurance and consumer user experience.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - From 256GB up to 2048GB
- **Electrical/Physical Interface**
  - PCIe Interface
  - Compliant with NVMe 1.3
  - PCIe Express Base Ver 3.1
  - PCIe Gen 3 x 4 lane & backward compatible to PCIe Gen 2 and Gen 1
  - 8 IO queues supported (1 admin queue and 8 IO queue). Each IO queue support 256 entries.
  - Support power management
- **Supported NAND Flash**
  - Support up to 32 Flash Chip Enables (CE) within a single design
  - Support up to 4/8pcs BGA132 flash
  - Support 8-bit I/O NAND Flash
  - Support ONFI 2.3, ONFI 3.0, ONFI 3.2 and ONFI 4.0 interface
    - Kioxia BiCS4 TLC
    - Kioxia BiCS5 TLC
- **ECC Scheme**
  - PS5012-E12 PCIe SSD applies LDPC of ECC algorithm.
- **Supported Sector size**
  - 512Bytes
- **GPIO**
- **Support SMART and TRIM commands**
- **LBA Range**
  - IDEMA standard
- **Certification & Compliance**
  - RoHS
  - WHQL
  - PCI Express Base 3.1
  - UNH-IOL NVM Express Logo

- **Security features**
  - FIPS 140-2 lv certified: when used in FIPS approved mode (When installed, initialized and configured as specified in the Security Rules Section of the Phison FIPS 140-2 non-proprietary Security Policy)
  - Full disk AES-XTS 256bit hardware encryption to protect user data storage
  - RSA-2048 Digital Signature Verification for secure boot and secure firmware update
  - On-chip Deterministic Random Number Generator used for key generation
  - Tamper-Evidence Protection
  - Support of TCG OPAL SSC 2.0

- **Weight**

Capacity	Flash Configuration	Flash Type	Weight (g)
256GB	64GBx4	BiCS4 TLC, 256Gb Die	8.5
512GB	128GBx4	BiCS4 TLC, 256Gb Die	8.5
1024GB	256GBx4	BiCS4 TLC, 256Gb Die	8.9
2048GB	512GBx4	BiCS4 TLC, 512Gb Die	9.2
256GB	128GBx2	BiCS5 TLC, 512Gb Die	7.5
512GB	128GBx4	BiCS5 TLC, 512Gb Die	8.4
1024GB	256GBx4	BiCS5 TLC, 512Gb Die	8.9
2048GB	512GBx4	BiCS5 TLC, 512Gb Die	9.0

- **TBW**

CTL	Capacity	Flash Type	TBW
E12	256GB	BiCS4 TLC, 256Gb Die	245
	512GB	BiCS4 TLC, 256Gb Die	545
	1024GB	BiCS4 TLC, 256Gb Die	1140
	2048GB	BiCS4 TLC, 512Gb Die	2310
	256GB	BiCS5 TLC, 512Gb Die	220
	512GB	BiCS5 TLC, 512Gb Die	550
	1024GB	BiCS5 TLC, 512Gb Die	1200
	2048GB	BiCS5 TLC, 512Gb Die	2470

NOTES:

1. Samples were built using Kioxia TLC.
2. TBW may differ according to flash configuration and platform.
3. The test followed JEDEC219A client endurance workload.
4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

- **Performance**

Form Factor	Capacity	Flash	Flash Type	Sequential		Random	
				Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
M.2 2280 Double Side (BiCS4)	E12 240, 256GB	64GB x 4	BGA132, BiSC4 TLC, 256Gb DDP	3300	1300	210K	320K
	E12 480, 512GB	128GB x 4	BGA132, BiSC4 TLC, 256Gb QDP	3400	2500	420K	625K
	E12 960, 1024GB	256GB x 4	BGA132, BiSC4 TLC, 256Gb ODP	3400	3100	640K	680K
	E12 1920, 2048GB	512GB x 4	BGA132, BiSC4 TLC, 512Gb ODP	3400	3000	635K	685K
M.2 2280 Double Side (BiCS5)	E12 240, 256GB	128GBx2	BGA132, BiSC5 TLC, 512Gb DDP	1900	1100	100K	280K
	E12 480, 512GB	128GBx4	BGA132, BiSC5 TLC, 512Gb DDP	3300	2300	200K	550K
	E12 960, 1024GB	256GBx4	BGA132, BiSC5 TLC, 512Gb QDP	3300	3100	400K	600K
	E12 1920, 2048GB	512GBx4	BGA132, BiSC5 TLC, 512Gb ODP	3300	3000	640K	630K

NOTES:

1. Performance was estimated based on Kioxia TLC.
2. Performance may differ according to flash configuration and platform.
3. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.
4. Performance is and measured with the following conditions
   (a) CrystalDiskMark 6.0.0, 1GB range, QD=32, Thread=1
   (b) IOMeter, 1GB range, 4K data size, QD=32

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

Table 3-1 High Temperature

	Temperature	Humidity
Operation	70°C	0% RH
Storage	85°C	0% RH

Table 3-2 Low Temperature

	Temperature	Humidity
Operation	0°C	0% RH
Storage	-40°C	0% RH

Table 3-3 High Humidity

	Temperature	Humidity
Operation	40°C	90% RH
Storage	40°C	93% RH

Table 3-4 Temperature Cycling

	Temperature
Operation	0°C
	70°C[1]
Storage	-40°C
	85°C

NOTES:

1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Shock

Table 3-5 Shock

	Acceleration Force
Non-operational	1500G

3.1.3. Vibration

Table 3-6 Vibration

	Condition	
	Frequency/Displacement	**Frequency/Acceleration**
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G

3.1.4. Drop

Table 3-7 Drop

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

3.1.5. Bending

Table 3-8 Bending

	Force	Action
Non-operational	≥ 20N	Hold 1min/5times

3.1.6. Durability

Table 3-9 Durability

	Condition
operational	1000 mating cycles

3.1.7. Electrostatic Discharge (ESD)

Table 3-10 ESD

Specification	+/-4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.8. EMI Compliance

Table 3-11 EMI

Specification
EN 55032, CISPR 32(CE)
AS/NZS CISPR 32(CE)
ANSI C63.4 (FCC)
VCCI-CISPR 32 (VCCI)
CNS 13438 (BSMI)

3.2. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is smaller in 1,800,000 hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage

Parameter	Rating
Operating Voltage	Min = 3.14V Max = 3.47 V
Rise Time (Max/Min)	100 ms / 0.1 ms
Fall Time (Max/Min)	5 s / 1 ms
Min. Off Time1	1 s

NOTE:

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.

4.2. Power Consumption

Table 4-2 Power Consumption in W

Capacity	Flash Configuration	CE#	Read		Write	
			Max.	Avg.	Max.	Avg.
E12 256GB	BGA132, BiCS4 TLC, 256Gb DDP	8	5.0	4.7	3.1	3.0
E12 512GB	BGA132, BiCS4 TLC, 256Gb QDP	16	5.1	4.9	4.5	4.4
E12 1024GB	BGA132, BiCS4 TLC, 256Gb ODP	32	5.3	5.3	5.2	5.1
E12 2048GB	BGA132, BiCS4 TLC, 512Gb ODP	32	5.3	5.0	5.7	5.6
E12 256GB	BGA132, BiSC5 TLC, 512Gb DDP	4	3.7	3.6	3.3	3.2
E12 512GB	BGA132, BiSC5 TLC, 512Gb DDP	8	5.2	5.2	4.7	4.6
E12 1024GB	BGA132, BiSC5 TLC, 512Gb QDP	16	5.3	5.3	5.5	5.4
E12 2048GB	BGA132, BiSC5 TLC, 512Gb ODP	32	5.5	5.5	5.9	5.8

NOTES:

1. Based on ECPM1x.x-series under ambient temperature.
2. Use CrystalDiskMark 6.0.0 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.

Table 4-3 Power Consumption in mW

Capacity	Flash Configuration	CE#	Active			PS3	PS4
			PS0	PS1	PS2		
E12 256GB	BGA132, BiCS4 TLC, 256Gb DDP	8	5000	1700	1700	16	2

E12 512GB	BGA132, BiCS4 TLC, 256Gb QDP	16	5100	1800	1700	16	2
E12 1024GB	BGA132, BiCS4 TLC, 256Gb ODP	32	5300	1900	1700	21	2
E12 2048GB	BGA132, BiCS4 TLC, 512Gb ODP	32	5700	1900	1800	22	2
E12 256GB	BGA132, BiSC5 TLC, 512Gb DDP	4	3700	2000	2000	16	2
E12 512GB	BGA132, BiSC5 TLC, 512Gb DDP	8	5200	2100	2000	16	2
E12 1024GB	BGA132, BiSC5 TLC, 512Gb QDP	16	5500	2000	2000	20	2
E12 2048GB	BGA132, BiSC5 TLC, 512Gb ODP	32	5500	2200	2100	33	2

NOTES:

1. Based on ECPM1x.x-series under ambient temperature.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.
4. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
5. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.

5. INTERFACE

5.1. Pin Assignment and Descriptions

Table 5-1 defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.

Figure 5-1 Pin Assignment and Description of PS5012 M.2 2280

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec

Pin No.	PCIe Pin	Description
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground

Pin NO.	PCIe Pin	Description
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

6. SUPPORTED COMMANDS

6.1. Command List

Table 6-1 Admin Commands

Identifier	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Feature
0Ah	M	Get Feature
0Ch	M	Asynchronous Event Request
0Dh	O	Namespace management (Not Supported)
10h	O	Firmware Commit
11h	O	Firmware Image Download
14h	O	Device Self-test (Not supported)
15h	O	Namespace Attachment (Not supported)
18h	O	Keep Alive (Not Supported)
19h	O	Directive Send (Not Supported)
1Ah	O	Directive receive (Not Supported)
1Dh	O	NVMe-MI Send (Not Supported)
1Eh	O	NVME-Mi Receive (Not Supported)
80h	O	Format NVM (disabled when in FIPS approved mode)
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize (disabled)

Table 6-2 I/O Commands

Identifier	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable (Not Supported)
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

Table 6-3 Set Feature Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type (Not Supported)
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number Of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer (Not supported)
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh - 7Dh		Reserved
80h	O	Software Progress Marker

Table 6-4 Get Log Page Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List (Not supported)
06h	O	Device Self-test (Not supported)
09h - 7Fh		Reserved
81h	-	Sanitize Status (not supported)
82h - FFh		Reserved

6.2. Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-5 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	-
63:24	M	Model Number (MN)	-
71:64	M	Firmware Revision (FR)	ECPM1x.x
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	*
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities(CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x01
83:80	M	Version (VER)	0x10300
87:84	M	RTD3 Resume Latency (RTD3R)	0x989680
91:88	M	RTD3 Entry Latency (RTD3E)	0x989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x200
99:96	M	Controller Attributes (CTRATT)	0x02
111:100		Reserved	0x00
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128		Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00

257:256	M	Optional Admin Command Support (OACS)	0x07
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x08
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x15C
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x161
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x64
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00
Bytes	**O/M**	**Description**	**Default Value**
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00
295:280	O	Total NVM Capacity (TNVMCAP)	256GB: 0x3B9E6560 512GB: 0x773C2560 1024GB: 0xEE77A560 2048GB: 0x01DCEEA560
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00
317:316	O	Extended Device Self-test Time (EDSTT)	0x00
318	O	Device Self-test Options (DSTO)	0x00
319	M	Firmware Update Granularity (FWUG)	0x01
321:320	M	Keep Alive Support (KAS)	0x00
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x01
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x139
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x157
331:328	O	Sanitize Capabilities (SANICAP)	0x00
511:332		Reserved	0x00

NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	M	Number of Namespaces (NN)	0x01
521:520	M	Optional NVM Command Support (ONCS)	0x5D
523:522	M	Fused Operation Support (FUSES)	0x00

524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	0xFF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x00
535:534	M	Reserved	0x00
539:536	O	SGL Support (SGLS)	0x00
767:540		Reserved	0x00

IO Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	0x00
1791:1024		Reserved	0x00
2047:1792	-	Refer to the NVMe over Fabrics specification	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	0x02A5
IO Command Set Attributes			
2111:2080	O	Power State 1 Descriptor (PSD1)	[2081:2080]0x023B [2095:2092]0x01010101
2143:2112	O	Power State 2 Descriptor (PSD2)	[2113:2112]0x0207 [2127:2124]0x02020202
2175:2144	O	Power State 3 Descriptor (PSD3)	[2147:2144]0x030001EA [2159:2156]0x03030303
2207:2176	O	Power State 4 Descriptor (PSD4)	[2179:2176]0x03000012 [2191:2188]0x04040404
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00

2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00

Vendor Specific			
4092:3072	O	Vendor Specific (VS)	Phison Reserved
4093	O	[Phison specific] Bit 0 : FIPS firmware Bit 1: FIPS mode	 0x01 0x03
4096:4094	O	Vendor Specific (VS)	Phison Reserved

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

** depends on the using of capacity

“-“depends on each sample

Table 6-6 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	256GB: 0x1DCF32B0 512GB: 0x3B9E12B0 1024GB: 0x773BD2B0 2048GB: 0xEE7752B0
15:8	M	Namespace Capacity (NCAP)	256GB: 0x1DCF32B0 512GB: 0x3B9E12B0 1024GB: 0x773BD2B0 2048GB: 0xEE7752B0
23:16	M	Namespace Utilization (NUSE)	256GB: 0x1DCF32B0 512GB: 0x3B9E12B0 1024GB: 0x773BD2B0 2048GB: 0xEE7752B0
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33		Reserved	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000

Bytes	O/M	Description	Default Value
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Reserved	0x0000
64:48	O	NVM Capacity (NVMCAP)	256GB: 0x3B9E6560 512GB: 0x773C2560 1024GB: 0xEE77A560 2048GB: 0x01DCEEA560
103:64		Reserved	0x00

119:104	O	Namespace Globally Unique Identifier (NGUID)	0x00
127:120	O	IEEE Extended Unique Identifier (EUI64)	TBD**
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192		Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

*See IDEMA SPEC

** See IEEE EUI-64 SPEC

Table 6-7 List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)	Byte[7:0]: Namespace Size (NSZE) (Dec)
256	1DCF32B0h	500,118,192
512	3B9E12B0h	1,000,215,216
1024	773BD2B0h	2,000,409,264
2048	EE7752B0h	4,000,797,360

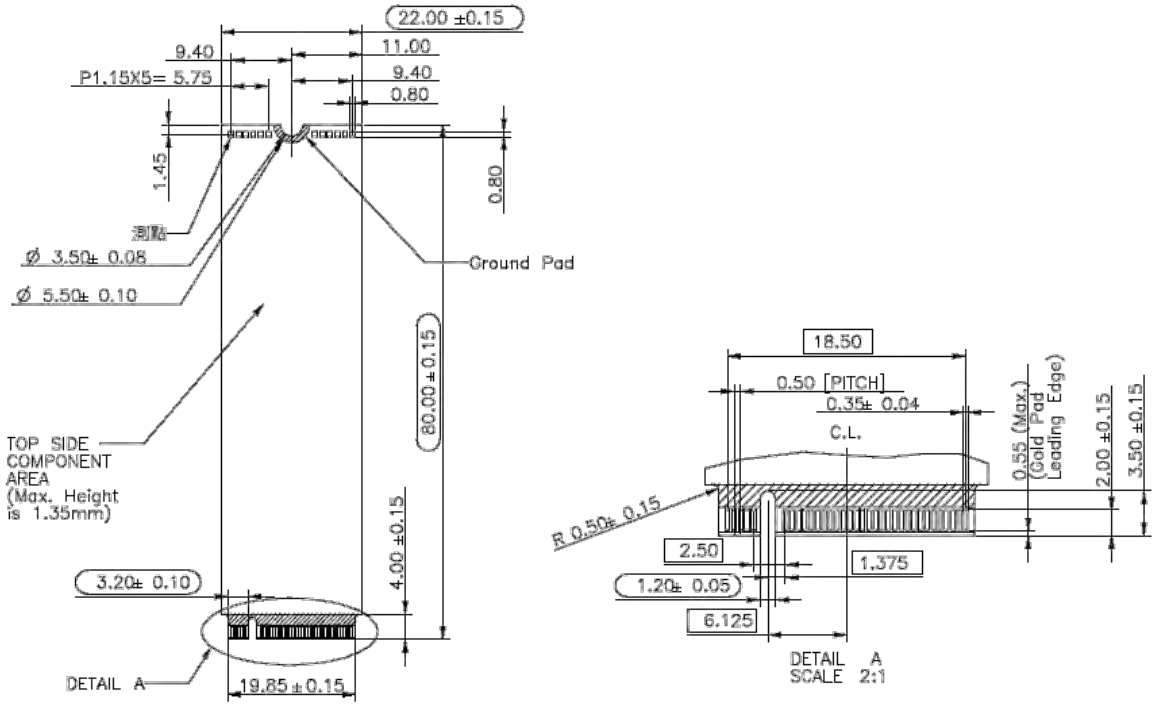
6.3. SMART Attributes

Table 6-8 SMART Attributes (Log Identifier 02h)

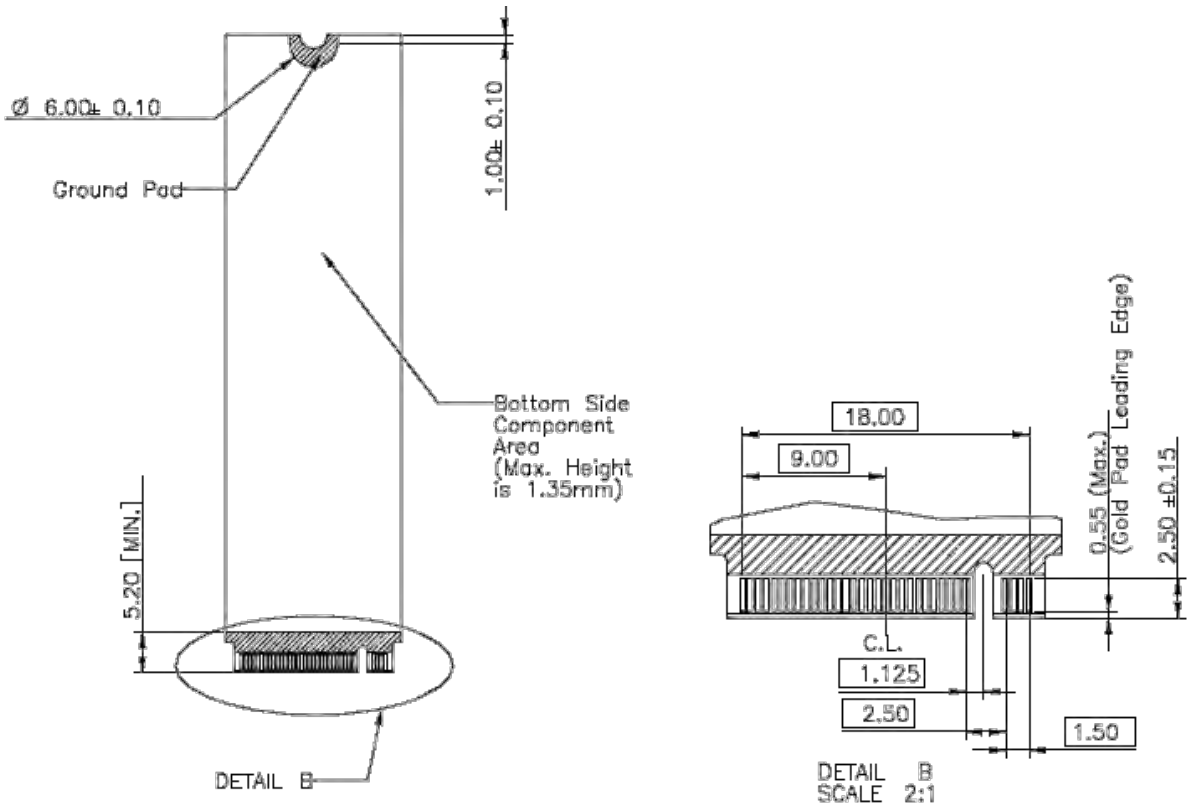
Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

7. PHYSICAL DIMENSION

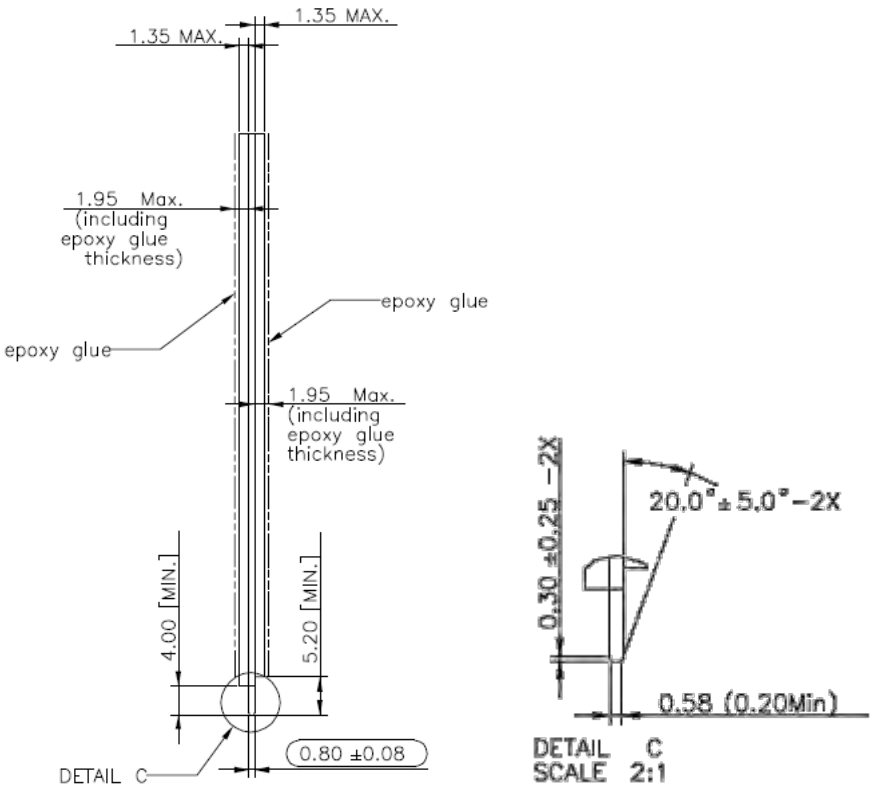
❖ Dimension of M.2 2280-D2-M : 80.00mm (L) x 22mm (W) x 3.5mm (H) / 4.7mm(w/epoxy)(H)



Top View



Bottom View


1.35 MAX.
1.35 MAX.
1.95 Max.
(including
epoxy glue
thickness)
epoxy glue
epoxy glue
1.95 Max.
(including
epoxy glue
thickness)
4.00 [MIN.]
5.20 [MIN.]
0.80 ±0.08
DETAIL C
0.30 ±0.25 -2X
20.0° ± 5.0° -2X
0.58 (0.20Min)
DETAIL C
SCALE 2:1

Side View

8. PRODUCT WARRANTY POLICY

For any other products manufactured and supplied by Phison (“Phison Products”), Phison hereby certify that in the event Phison Product does not conform to the specification for (A) a period instructed by Phison or mutually agreed by Phison and the customer in writing or (B) the period ending on the date at which customer’s use of a Phison Product exceeds Phison Product’s total Terabytes Written as recorded by or derived from Phison Product’s S.M.A.R.T. Attribute, including but not limited to, Phison Product’s drive life is used up in accordance with the S.M.A.R.T. Attribute, whichever occurs earlier(“Warranty Period”) and such inconformity is confirmed by Phison to be solely attributable to Phison agrees to repair or replace the nonconforming Phison Product, free of charge.

Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

(1) alternation, modification, improper use, misuse or excessive use of Phison Product;

(2) failure to comply with Phison’s instructions;

(3) Phison’s compliance with or use of the instructions, technologies, designs, specifications, devices, materials, components, parts, software and firmware provided, instructed or approved by Buyer (including any of its parents, subsidiaries, affiliates, suppliers, subcontractors or downstream customers);

(4) combination of Phison Product with other materials, components, parts, goods, hardware, firmware or software not supplied by Phison;

(5) any claim brought by a third party who is commonly known as intellectual property right assertion entity or patent troll;

(6) NAND flash itself or NAND flash which is embedded into Phison Products;

(7) Phison’s compliance with general industry standards;

(8) other error or failure not solely attributable to Phison’s cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

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9. REFERENCE

The following table is to list out the standards that have been adopted for designing the product.

Table 9-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at sales@phison.com or support@phison.com.
M.2	http://www.pcisig.com
PCI Express Base 3.0	https://www.pcisig.com/specifications/pciexpress/base3/
NVM Express Specification Rev.1.3	http://www.nvmexpress.org/
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a

10. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 10-1 List of Terminology

Term	Definitions
DDR	Double data rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical block addressing
MB	Mega-byte
GB	Giga-byte
TB	Tera-byte
MTBF	Mean time between failures
PCIe	PCI Express / Peripheral Component Interconnect Express
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk